

Abstract

An apparatus and method for noise reduction in a successive approximation (SA) analog-to-digital converter (ADC) is provided. The SA ADC includes a noise-compensating comparator circuit, an SA logic circuit, and a DAC circuit. A first reference signal is generated such that the first reference signal has a noise component that is substantially similar to a noise component of a first comparison signal. The noise-compensated comparator circuit is configured to provide a differential signal. The first comparison signal is included in a first half of the differential signal, and the first reference signal is included in a second half of the differential signal, such that the noise component of the first comparison signal is substantially cancelled out differentially. The noise-compensating comparator circuit is further configured to compare the two halves of the differential signal to provide a comparator output signal.